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PATENT APPLICATION

ATTORNEY DOCKET NO. 200301968-2

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): David W. Hartwell

Confirmation No.: 2641

Application No.: 09/944,500

Examiner: Torres, Juan A.

Filing Date: 08/31/2001

Group Art Unit: 2631

Title: DETECTION OF ADDED OR MISSING FORWARDING DATA CLOCK SIGNALS

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on 12/07/2005.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Number of pages: **16**

Typed Name: **Melissa Altman**

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Respectfully submitted,

David W. Hartwell

By Michael R. Reinemann

Michael R. Reinemann

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PATENTS
15311-2312
200301968-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re The Application of:
David W. Hartwell

Serial No.: 09/944,500

Filed: August 31, 2001

For: Detection of Added or Missing Forwarding Data Clock Signals

Examiner: Torres, Juan A.

Art Unit: 2631

Cesari and McKenna, LLP
88 Black Falcon Avenue
Boston, MA 02210
February 2, 2006

CERTIFICATE OF MAILING

I hereby certify that the following papers are being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 2, 2006.

Melissa L. Altman

_X_ Appeal Brief
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Melissa Altman

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

APPEAL BRIEF

In response to the Notice of Appeal mailed December 7, 2005, Applicant hereby submits this Appeal Brief.

REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, L.P. of Houston, Texas.

RELATED APPEALS AND INTERFERENCES

Applicant and its legal representatives know of no related appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in the present appeal.

STATUS OF CLAIMS

Claims 1-16 are pending in the case. Claims 1-3, 5-7 and 9-16 stand twice rejected under 35 U.S.C. §102(e), and claims 4 and 8 stand twice rejected under 35 U.S.C. §103.

A copy of claims 1-16, in their current form, is attached hereto as an Appendix.

STATUS OF AMENDMENTS

No amendments have been filed since the mailing of the Final Rejection on October 21, 2005.

SUMMARY OF CLAIMED SUBJECT MATTER

The summary is set forth in three exemplary embodiments that correspond to independent claims 1, 5, and 9, and dependent claims 2, 6, and 14. Discussions about elements and recitations of these claims can be found at least at the cited locations in the specification and drawings.

Independent claim 1 is directed to an error detection system for a clock signal. The system includes a first counter (48) that counts a clock signal (18), a phase-locked loop circuit (48) that receives the clock signal and outputs a second clock signal, a second counter

(52) that counts this second clock signal, a comparator (54) that compares the two counters (46, 52), and an error output (56) that is true when the counts of the two counters (46, 52) are unequal. See Specification at pp. 5-6.

Independent claim 5 is directed to a method of detecting clock signal errors. The method recites counting a first clock signal, providing a second clock signal with a frequency that is locked to the average frequency of the first clock signal, counting this second clock signal, detecting a difference between the first and second counts, and signaling an error therewith. See Specification at pp. 5-6.

Independent claim 9 is directed to a system for detecting errors in a first clock signal. The system includes means for counting a first clock signal (e.g., counter 46), means responsive to the first clock signal for generating a second clock signal (e.g., phase-locked loop 48), means for counting the second clock signal (e.g., counter 52), means for comparing the two counts (e.g., comparator 54), means for generating an error when the count of the first and second clock signals differs (e.g., error signal 56). See Specification at pp. 5-6.

Claim 2 depends from system claim 1 and recites that the comparator has a second output that indicates which counter contains the higher count. See Specification at p. 5.

Claim 6 depends from method claim 5 and adds the step of step of signalling which count is higher. See Specification at p. 5.

Claim 14 depends from system claim 6 and recites means for determining (e.g., comparator 54) whether the count of the first clock signal is higher or lower than the count of the second clock signal. See Specification at pp. 5 and 7, and Fig. 4.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1, 5 and 9, which otherwise meet all conditions of patentability under Title 35 of the United States Code, are unpatentable under 35 U.S.C. §102(e) over U.S. Pat. No. 6,314,150 to Vowe ("Vowe")[1], where Vowe fails to disclose, among other things, an error detection system having a phase-locked loop (PLL) that generates a second clock signal based upon a first clock signal, or counters for counting both the first clock signal and the second clock signal, among other deficiencies.

Whether claims 2, 6 and 14, which otherwise meet all conditions of patentability under Title 35 of the United States Code, are inherently unpatentable under 35 U.S.C. §102(e) over Vowe, where Vowe fails to disclose either expressly or inherently a comparator having a second output to indicate which of the two counts being compared is higher.

ARGUMENT

Legal Standard

Anticipation is established only when a single prior art reference discloses each and every element of a claimed invention united in the same way. RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444 (Fed. Cir. 1984). There can be no difference between the claimed invention and the cited reference, as viewed by a person of ordinary skill in the art. Scripps Clinic & Research Foundation v. Genentech Inc., 927 F.2d 1565, 1576 (Fed. Cir. 1991). The burden of establishing a prima facie case of anticipation rests with the examiner, who must show where each limitation of the claims is found in the prior art refer-

[1] The final Office Action refers to Vowe as U.S. Pat. No. 6,114,917. However, Vowe is actually U.S. Pat. No. 6,314,150. The patent number identified by the Examiner, Patent No. 6,114,917 refers to another reference cited against the present application.

ence. If a single claim limitation is missing from the prior art reference, then the rejection is improper and should be withdrawn or reversed.

The claims do not stand or fall together. Instead, Applicant presents separate arguments for various independent and dependent claims. Each of these arguments is separately argued below and presented with separate headings and sub-headings as required by 37 C.F.F. §41.37(c)(1)(vii).

Description of the Cited References

Vowe discloses a lock detector (LD) circuit for use within a phase-locked loop (PLL) to indicate whether the PLL is currently locked or not locked. Vowe's LD circuit receives two signals, TA and TB. See Fig. 2. TA is a divided-down output signal of the phase-locked loop. See Col. 5, lines 48-50 ("The first input clock signal TA may be, for example, the divided-down output clock signal of the phase-locked loop"). TB is a reference clock signal generated by a crystal oscillator. See Col. 5, lines 50-52 ("The second input clock signal TB is the reference clock signal, which is generated by a crystal oscillator, for example"). Vowe's TA and TB signals are coupled to corresponding counters, ZA and ZB. See Col. 5, lines 52-54. Counter signals from the two counters, ZA and ZB, and then provided to two comparators VA, VB. See Col. 5, lines 63-66. The two comparators VA and VB generate respective LOCK signals, LOCK_A and LOCK-B, which are then ANDed to generate the final LOCK signal for the LD circuit. See Col. 6, lines 5-11.

Claim 1

Claim 1 in relevant part recites:

"An error detection system for **a clock signal** comprising:

a first counter that receives and counts the clock signal,

a phase-locked loop circuit **that receives the clock signal and outputs a second clock signal,**

a second counter that receives and counts the second clock signal,

a comparator that receives and compares the outputs of the first and the second counters".

As shown, claim 1 explicitly recites that a phase-locked loop (PLL) circuit receives a first clock signal, and then outputs a second clock signal, and that the two counters count the first clock signal, i.e., the input signal to the PLL, and the second clock signal, i.e., the output of the PLL. Such an arrangement is nowhere disclosed in Vowe.

In particular, with Vowe, the first counter, ZA, receives a divided down output from a PLL. See Col. 5, lines 48-50 ("The first input clock signal TA may be, for example, the divided-down output clock signal of the phase-locked loop"). Rather than receiving the same input signal as the one being fed to the PLL, as recited in claim 1, however, Vowe's second counter, ZB, receives **a reference signal** generated by a crystal oscillator. See Col. 5, lines 50-52 ("The second input clock signal TB is the reference clock signal, which is generated by a crystal oscillator, for example").

Vowe provides no disclosure of connecting the input signal that drives the PLL to its counter ZB. As shown in the Background section, Vowe knows how to use language that identifies the PLL's input signal. See Col. 1, lines 14-15 ("Phase-locked loops (PLL) are used to correct frequency differences between an *input signal* and a comparison signal"). Notwithstanding this use of "input signal" in the Background, Vowe makes clear that it is a different signal, a reference signal, that is coupled to its ZB counter. See Col. 5, lines 50-52.

The final Office Action equates Vowe's two counters, ZA and ZB, with Applicant's claimed counters. See Final Office Action at p. 5. However, as shown above, Vowe provides no disclosure of a first counter that receives the same input as a PLL, and a second counter that receives the output of the PLL. In fact, there is no PLL shown in any of Vowe's drawings.

For these reasons, Applicant submits that Vowe fails to disclose each and every element of claim 1 in the manner recited therein. Accordingly, Applicant requests that the rejection of claim 1 as being anticipated by Vowe be reversed.

Claims 5 and 9

Independent claims 5 and 9 are also distinguishable over Vowe. In particular, claim 5 in relevant part recites:

> "A method for detecting clock signal errors comprising the steps of:"
>
> "a first counting of the first clock signals",
>
> "providing a second clock signal with a frequency that is locked to the average frequency of the first clock signal", and
>
> "a second counting of the second clock signals".

As shown above, Vowe fails to disclose a method where a first signal and a second signal, whose frequency is locked to the average frequency of the first clock signal, e.g., by a PLL, are both counted. Instead, Vowe discloses a Lock Detector circuit that counts a divided down output of a PLL, and a reference signal produced by a crystal oscillator.

Similarly, claim 9 in relevant part recites:

> "A system for detecting errors in a first clock signal, the system comprising:"
>
> "means for counting the first clock signal,"

"means, **responsive to the first clock signal**, for generating a second clock signal", and

"means for counting the second clock signal".

Again, Vowe fails to disclose system that counts both a first signal and a second signal generated in response to the first signal, e.g., by a PLL. Accordingly, the rejections of claims 5 and 9 based on Vowe should be reversed.

Claim 2

Claim 2 recites:

"The error detection system as defined in claim 1 further comprising **a second output from the comparator that indicates which counter contains a higher count**."

In rejecting claim 2, the final Office Action, at p. 6, cites to Vowe Fig. 2 (blocks VA and VB) and Col. 4, line 66 to Col. 7, line 6.

Vowe, however, fails to disclose a second output from a comparator that indicates which counter is higher. Instead, Vowe only discloses that its two comparators, VA and VB, output a Boolean indication (i.e., a "1" or a "0"), and a reset signal (i.e., RESET_A and RESET_B). See Col. 6, lines 5-15. These Boolean values are then ANDed by Vowe's selection device to produce the final LOCK signal. See Col. 6, lines 10-11. Vowe provides no disclosure for a comparator that includes, as one of its outputs, an indication as to which of two different counters had a higher count.

At pp. 4-5, the final Office Action contends that "Vowe inherently discloses an output from the comparator that indicates which counter contains a higher count using the VA and VB comparators with different thresholds."

Applicant submits that the final Office Action fails to satisfy its burden in rejecting claim 2 based on inherency.

To establish inherency, extrinsic evidence

> must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.

In re Robertson, 169 F.3d 743, 745 (Fed. Cir. 1999).

Here, no extrinsic evidence has been cited in the final Office Action in support of the contention that Vowe's comparator inherently provides, as an output, an indication of which counter contains a higher count.

Furthermore, the final Office Action's argument, that it is inherent to set the threshold used by Vowe's comparator VA to zero, and that by doing so one somehow achieves the Applicant's invention, is wrong. Specifically, the final Office Action refers to Col. 6, line 66 to Col. 7, line 6, where Vowe states that if the difference between counts ZA and ZB exceeds a predetermined threshold, then the comparator VA sets its LOCK_A signal to 0. This effectively forces Vowe's the lock detector (LD) circuit to produce a non-locked output.

If this threshold were set to zero, as suggested in the final Office Action, then it would simply cause Vowe's LD circuit to produce a non-locked output condition whenever the two counts ZA and ZB were different. It would not produce any indication as to which counter is higher, nor would it somehow cause comparator VA to produce an output to that effect, especially where Vowe's comparator VA lacks the capability to produce such an output.

Accordingly, Applicant submits that the inherency rejection of claim 2 is improper, and should be reversed.

Claims 6 and 14

Dependent claim 6 recites "the step of: signalling which counting is higher".

Similarly, dependent claim 14 recites "means for determining whether the count of the first clock signal is higher or lower than the count of the second clock signal."

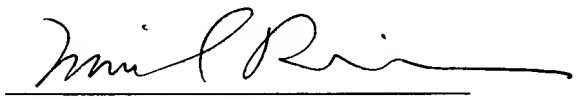
As explained above, Vowe fails to disclose either expressly or inherently either (i) a signal indicating which count is higher, or (ii) means for determining which count is higher.

Accordingly, Applicant submits that the rejections of claims 6 and 14 should also be reversed.

CONCLUSION

Applicant respectfully submits that the claims are allowable over the art of record. Accordingly, Applicant requests that the rejection of all claims be reversed.

Respectfully submitted,



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CLAIMS APPENDIX
(Claims on Appeal in Appl. Ser. No. 09/944,500)

1. (Previously presented) An error detection system for a clock signal comprising:

a first counter that receives and counts the clock signal,

a phase-locked loop circuit that receives the clock signal and outputs a second clock signal,

a second counter that receives and counts the second clock signal,

a comparator that receives and compares the outputs of the first and the second counters, and

an error output from the comparator that is true when the counts of the first and second counters are unequal.

2. (Previously presented) The error detection system as defined in claim 1 further comprising a second output from the comparator that indicates which counter contains a higher count.

3. (Original) The error detection system as defined in claim 1 further comprising means for resetting the counters synchronized to the successful capture of the clock signal by the PLL.

4. (Previously presented) The error detection system as defined in claim 1 further comprising:

a sender that sends data and the clock signal, the clock signal defined as a forwarding source synchronous clock signal, and

a receiver latch that accepts and latches the data therein with the forwarding clock.

5 (Original) A method for detecting clock signal errors comprising the steps of:

a first counting of the first clock signals,

providing a second clock signal with a frequency that is locked to the average frequency of the first clock signal,

a second counting of the second clock signals,

detecting a difference between the first and the second countings, and

signaling an error therewith.

6. (Original) The method as defined in claim 5 further comprising the step of: signalling which counting is higher.

7 (Previously presented) The method as defined in claim 5 further comprising the step of synchronizing the two countings.

8. (Original) The method as defined in claim 5 further comprising the steps of:

sending data and the clock signal, wherein the clock signal is a forwarding source synchronous clock signal,

receiving the data, and

latching the data with the forwarding clock signal.

9. (Previously presented) A system for detecting errors in a first clock signal, the system comprising:

means for counting the first clock signal,

means, responsive to the first clock signal, for generating a second clock signal,

means for counting the second clock signal,

means for comparing the count of the first clock signal with the count of the second clock signal, and

means for generating an error when the count of the first clock signal differs from the count of the second clock signal.

10. (Previously presented) The system of claim 9 wherein

the first clock signal has an average frequency, and

the second clock signal is locked to the average frequency of the first clock signal.

11. (Previously presented) The system of claim 9 wherein

the first clock signal has a plurality of rising edges and a plurality of falling edges, and

the means for counting the first clock signal counts one of the rising and falling edges.

12. (Previously presented) The system of claim 9 wherein

the first clock signal has a plurality of rising edges and a plurality of falling edges, and

the means for counting the first clock signal counts both the rising and falling edges.

13. (Previously presented) The system of claim 10 wherein the means for generating a second clock signal includes a phase lock loop (PLL) circuit.

14. (Previously presented) The system of claim 9 further comprising means for determining whether the count of the first clock signal is higher or lower than the count of the second clock signal.

15. (New) The system of claim 14 wherein the means for generating a second clock signal includes a phase lock loop (PLL) circuit.

16. (New) The system of claim 14 wherein

the first clock signal has an average frequency, and

the second clock signal is locked to the average frequency of the first clock signal.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.